

DISPLAY CONTROL CIRCUIT

Publication number: JP8036375

Publication date: 1996-02-06

Inventor: IMAMURA YOICHI; YAMAZAKI TAKU

Applicant: SEIKO EPSON CORP

Classification:

- International: G02F1/133; G09G3/36; G02F1/13; G09G3/36; (IPC1-7): G09G3/36; G02F1/133

- European:

Application number: JP19950012557 19950130

Priority number(s): JP19950012557 19950130

Report a data error here

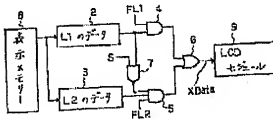
Abstract of JP8036375

PURPOSE: To make display ample with three-dimensional feel, perspective feel and shading feel having depth by providing respective display layers with priority functions.

CONSTITUTION: Blocks 2, 3 have functions to successively read on/off information from a display memory 8 of the addresses

corresponding to the respective layers, to latch this information, to convert the display memory data to the data receivable by an LCD module 9 and to successively deliver the data. The output of the block 2 is regulated by the signal FL1 which is generated by an AND GATE 4.

On the other hand, the output of the block 3 is regulated by the signal FL2 which is generated by an AND gate 5 and is simultaneously regulated by the output of a NAND gate 7 as well which imparts the display priority order between the layers. Then, the output of the gate 7 attains '0' in the case that the signal for controlling priority of the layer is S=1 at the timing at which the information of dot lighting is emitted from the block 2 and, therefore, the display information of the layer L2 emitted from the block 3 is disregarded by the gate 5 which receives the output of the gate 7 as its input.



Data supplied from the esp@cenet database - Worldwide